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IMAGE SIGNAL PROCESSING SYSTEM

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(71) Applicant: Hitach, Ltd.

(72) Inventor: Hideyuki Tsuji

(72) Inventor: Keisuke Nakajima

(72) Inventor: Yasuyuki Kojima

[Title of the Invention] IMAGE SIGNAL PROCESSING SYSTEM

[Abstract]

[Object] An object of the invention is to provide an image signal processing system which uses a buffer memory (3) or similar memory having a relatively small storage capacity and obtains a binary image signal of a high-quality pseudo halftone image with a simple arrangement.

[Structure] An image signal processing system for converting halftone image information into a binary image signal by using an error diffusion scheme includes binarization means (7) for parallelly binarizing pieces of halftone image information of a plurality of pixels that are adjacent to each other, a plurality of error generation means (8, 9) for obtaining errors in the binarization of the respective pixels, average value means (10) for averaging the binarization errors from the plurality of error generation means (8, 9), storage means (3, 4) for storing the averaged binarization error, and feedback means (12 - 14) for feeding back the output from the storage means (3, 4) to each input of the binarization means (7).

[What is Claimed Is:]

[Claim 1] An image signal processing system for converting halftone image information into a binary image signal by using an error diffusion scheme, characterized by comprising binarization means for binarizing halftone image information of each pixel, error generation means for obtaining an error in the binarization, storage means for storing upper bits of the binarization error obtained by said error generation means, latch means for latching lower bits of the binarization error, and feedback means for feeding back outputs from said storage means and said latch means to an input of said binarization means.

[Claim 2] The image signal processing system according to claim 1, characterized in that conversion means for bit-compressing the binarization error is arranged between said error generation means and said storage means, and inverse conversion means for bit-expanding the compressed binarization error is arranged on an output side of said storage means.

[Claim 3] An image signal processing system for converting halftone image information into a binary image signal by using an error diffusion scheme, characterized by comprising binarization means for parallelly binarizing pieces of halftone image information of a plurality of pixels that are adjacent to each other, a plurality of error generation means

for obtaining errors in the binarization of the respective pixels, average value means for averaging the binarization errors from said plurality of error generation means, storage means for storing the averaged binarization error, and feedback means for feeding back an output from said storage means to each input of said binarization means.

[Claim 4] The image signal processing system according to claim 2, characterized by comprising storage means for storing upper bits of the averaged binarization error, latch means for latching lower bits of the averaged binarization error, and feedback means for feeding back outputs from said storage means and said latch means to each input of said binarization means for parallelly binarizing the pieces halftone image information of the two pixels.

[Claim 5] An image signal processing system for converting halftone image information into a binary image signal by using an error diffusion scheme, characterized by comprising binarization means for binarizing halftone image information of each pixel, error generation means for obtaining an error in the binarization, storage means for storing the binarization error obtained by said error generation means, and feedback means for feeding back an output from said storage means to said binarization means through an error distributor, wherein when binarization

errors obtained from neighboring pixels around halftone image information derived from a pixel of interest are to be distributed, said error distributor expresses each of the binarization errors generated from the neighboring pixels by a binary number, assigns a specific bit of the binary number to each of the neighboring pixels in accordance with a position of the neighboring pixel, and adds the assigned bits to define a distribution amount.

[Claim 6] An image signal processing system for converting halftone image information into a binary image signal by using an error diffusion scheme, characterized by comprising binarization means for binarizing halftone image information of each pixel, error generation means for obtaining an error in the binarization, latch means for latching the binarization error obtained by said error generation means, feedback means for feeding back an output from said latch means to said binarization means, and correction means for increasing a halftone reproducibility in a sub scanning direction.

[Claim 7] The image signal processing system according to claim 6, characterized in that said correction means comprises means for applying an AC bias whose polarity is converted for at least each line to the input halftone image information.

[Claim 8] The image signal processing system

according to claim 6, characterized in that said correction means comprises storage means for storing a binary image signal obtained by said binarization means and feedback means for feeding back an output from said storage means to the input halftone image information.

[Claim 9] The image signal processing system according to claim 3 or 4, characterized in that said binarization means for parallelly binarizing the pieces of halftone image information of the plurality of pixels includes addition means for obtaining a sum value of pieces of halftone image information from adjacent pixels and comparison means for comparing an output value from said addition means with a threshold value.

[Claim 10] The image signal processing system according to any one of claims 1, 2, 5, and 6, characterized in that said binarization means for binarizing the halftone image information of each pixel includes storage means for storing an output binary image signal, prediction means for predicting a next binary image signal from an output from said storage means, and selection means for selectively outputting one of constants 0 and 1 and the binary image signal from said prediction means, and an output from said selection means is selected in accordance with a value of the input halftone image signal.

[Claim 11] The image signal processing system

according to claim 8, characterized by comprising encoding means for encoding the binary image signal obtained by said binarization means by using, as reference data, the output from said storage means for storing the binary image signal obtained by said binarization means.

[Claim 12] The image signal processing system according to claim 10, characterized by comprising encoding means for encoding the binary image signal obtained by said binarization means by using, as reference data, the output from said storage means for storing the output binary image signal.

[Claim 13] The image signal processing system according to claim 10, characterized by comprising comparison means for comparing the binary image signal from said binarization means for binarizing the halftone image information of each pixel with an output from said prediction means for predicting the next binary image signal, and encoding means for encoding an output binary signal from said comparison means.

[Claim 14] The image signal processing system according to claim 10, characterized by comprising comparison means for comparing the binary image signal from said binarization means for binarizing the halftone image information of each pixel with an output from said prediction means for predicting the next binary image signal, and encoding means for encoding an

output binary signal from said comparison means, and further comprising decoding means for decoding an encoded signal from said encoding means, selection means for generating the decoded binary image signal in response to an output from said decoding means, storage means for storing the decoded binary image signal, and prediction means for predicting a next binary image signal from an output from said storage means, wherein an output binary image signal from said prediction means is supplied to said selection means to cause said selection means to generate the original binary image signal that is decoded.

[Detailed Description of the Invention]

[0001]

[Industrial Field of Utilization]

The present invention relates to an image signal processing system and, more particularly, to an image processing apparatus which converts halftone image information for each pixel, which is obtained by scanning, into a binary image signal by using an error diffusion scheme and further executes processing such as encoding for the binary image signal.

[0002]

[Prior Art]

Conventionally, an error diffusion method is known as one of methods of converting halftone image information for each pixel, which is obtained by

scanning, into a binary image signal and, more particularly, methods of obtaining a binary image signal while maintaining the gray level held by original halftone image information. In the error diffusion method, halftone image information for each pixel is sequentially converted into a binary image signal, and an error generated upon conversion is distributed to the points of pixels where the halftone image information has not been converted into a binary image signal yet. With this processing, errors at the points of the respective pixels in binarization are canceled. The gray level of the original halftone image information is maintained in the obtained binary image signals.

[0003]

Fig. 23 is a view showing the schematic arrangement of a binarization circuit which uses the conventional error diffusion method. Fig. 24 is a view showing a state wherein errors from neighboring pixels are distributed in the error diffusion method.

[0004]

Referring to Fig. 23, reference numeral 200 denotes a binarizer; 201, an adder; 202, a buffer memory; 203, an error filter; and 204, an adder.

[0005]

When the screen shown on the left side of Fig. 23 is scanned, halftone image information corresponding to

each pixel is obtained. On the screen, main scanning from the left side to the right side and sub scanning from the upper side to the lower side are performed. More specifically, main scanning processing is performed from the left side to the right side of each line of the screen. When the main scanning processing is ended, main scanning processing for the line immediately below is started.

[0006]

The binarizer 200 binarizes received halftone image information and generates a binary image signal at the output. The adder 201 compares the input and output of the binarizer 200. Every time comparison is executed, the adder 201 generates an error upon binarization and supplies it to the buffer memory 202. The buffer memory 202 already stores binarization errors for pixels that have already undergone binarization. The error filter 203 calculates the weighted mean of the stored binarization errors. The resultant value is added to the halftone image information through the adder 204. This sum value is the distribution value to the halftone image signal.

[0007]

The binarization errors are distributed as shown in Fig. 24. A hatched pixel is a pixel of interest, which should be binarized now. Four neighboring pixels around the pixel of interest have already undergone

binarization. Binarization errors obtained in the four neighboring pixels are multiplied by weighting coefficients a, b, c, and d, respectively. The sum of the products is distributed to the pixel of interest. The weighting coefficients a, b, c, and d have a relation given by a + b + c + d = 1.

[0008]

In this binarization circuit, binarization errors obtained for the respective pixels by the adder 201 must be stored in the buffer memory 202. Hence, the buffer memory 202 must be a line memory having a storage capacity corresponding to a length almost equal to the number of pixels (or an integer multiple of the number of pixels) in the main scanning direction. In addition, to distribute a binarization error obtained in one pixel to even pixels adjacent in the sub scanning direction, a line memory is indispensable.

[0009]

As another method of obtaining a binary image signal while maintaining gray level held by original halftone image information, a method using delta-sigma modulation is known. This method is disclosed in, e.g., "Facsimile Transmission of Image with Gray Level by Δ-Σ Modulation", Proceedings of the 1973 IECE National Conference, p. 1023, and Japanese Patent Laid-Open Nos. 58-151776 and 61-152163. The error diffusion method and delta-sigma modulation have the

following similarity.

[0010]

Fig. 22(a) is a block diagram showing the schematic arrangement of a delta-sigma modulation circuit. Fig. 22(b) is a block diagram showing a circuit equivalent to the schematic arrangement. Referring to Fig. 22(b), a delay device 211 replaces the two-dimensional weighted mean circuit constituted by the buffer memory 202 and error filter 203 shown in Fig. 23.

[0011]

Referring to Fig. 22(a), reference numeral 205 denotes a binarizer; 206, an integrator; 207, a delay device; and 208, an adder.

[0012]

Let Q(z) be the generated quantization noise, and Y(z) be the output. The relationship between the input and the output of the delta-sigma modulation circuit is given by

[0013]

$$Y(z) = X(z) + (1 - z^{-1})Q(z) \qquad \text{...(Equation 1)}$$

where z^{-1} represents a delay.

[0014]

In the error diffusion circuit shown in Fig. 23, let X(z1,z2) be the input, Q(z1,z2) be the quantization noise generated by the binarizer 200, and Y(z1,z2) be the output. The relationship between the input and the

output is given by

[0015]

$$Y(z_1,z_2) = X(z_1,z_2) + (1 - H(z_1,z_2))Q(z_1,z_2)$$

$$H(z_1,z_2) = az_1^{-1} + bz_1^{-1}z_2^{-1} + cz_2^{-1} + dz_1z_2^{-1} \quad \text{...(Equation 2)}$$

where

a, b, c, and d are the coefficients of the error filter; a + b + c + d = 1

z_1^{-1} and z_2^{-1} are delays in the main scanning direction and in the sub scanning direction, respectively.

[0016]

That is, in the error diffusion method, delta-sigma modulation is two-dimensionally extended. Conversely, a binarization scheme using delta-sigma modulation can be regarded as a special case wherein binarization errors are distributed only in the main scanning direction by the error diffusion method.

[0017]

Generally, when a person looks at an image, fine parts, i.e., the high-frequency components of the image are attenuated by a visual smoothing function and become unnoticeable. As is apparent from Equations 1 and 2, in the error diffusion method or delta-sigma modulation, the frequency components of quantization noise are concentrated on high-frequency components. That is, in the binarization scheme using the error

diffusion method or delta-sigma modulation, quantization noise is concentrated on frequency components that are unnoticeable because of the visual characteristic, thereby realizing pseudo halftone expression.

[0018]

In addition, various image signal processing systems of converting halftone image information into a binary image signal by using an error diffusion scheme or encoding the binary image signal are already known. For example, in a system disclosed in Japanese Patent Laid-Open No. 1-284172, a binarization error between halftone image information and a binary image signal is obtained and then weighted. The resultant error is distributed to neighboring pixels. In addition, the remainder of the error, which is obtained by weighting, is corrected, thereby increasing the density consistency between the halftone image information and the binary image signal. In a system disclosed in Japanese Patent Laid-Open No. 2-182080, when halftone image information from a pixel of interest should be converted into a binary image signal, binarization is executed while referring to the binary image signals of already binarized pixels on the line immediately before the line on which the pixel of interest is present, or the binary image signals of already binarized pixels on the line on which the pixel of interest is present.

Subsequently, the binary image signal is encoded to decrease the data amount of the binary image signal.

[0019]

[Problems That the Invention Is to Solve]

In converting halftone image information into a binary image signal by using the conventional error diffusion method, halftone image information obtained from each pixel is sequentially binarized, and a binarization error generated at this time is distributed to a pixel that has not been binarized yet. This method poses the following problems.

[0020]

As the first problem, every time a pixel is to be binarized, binarization errors need to be read out from the buffer memory or written in the buffer memory. For this reason, the processing speed is limited depending on the memory access time. To eliminate this limitation, a plurality of data are processed by increasing the bus width. In addition, the buffer memory is prepared in the LSI. However, this leads to large-scale hardware, resulting in high cost.

[0021]

As the second problem, as information to be used to binarize a pixel, only information held by the pixel itself and information of already binarized pixels can be used. Hence, even though the gray level in a wide range of the screen is maintained, binarization of the

individual pixels is not always optimum. More specifically, even when the values of halftone image information from two adjacent pixels a and b have a relationship a > b, 0 may be assigned to the pixel a while 1 may be assigned to the pixel b. For example, when the value of the pixel a is slightly smaller than the threshold value, 0 is assigned to the pixel a. Part of the binarization error is carried to the next pixel b. Hence, even when a > b, if "value b of pixel b + (error)" is larger than the threshold value, the pixel b is 1. Such a phenomenon disturbs the edge portions or thin line portions of the screen. To solve such a problem, Japanese Patent Laid-Open No. 61-32654 and "Pseudo Halftone Reproduction Processor Using Peripheral Density Integration Re-Distribution Method (CAPIX Method)", transactions of IIEEJ, Vol. 17, No. 5 (1988) pp. 361-368 disclose binarization schemes, in which a window having an appropriate size on the screen is scanned. A sequence is assigned to pieces of halftone image information obtained at the respective pixels in this window. Black pixels are laid out in accordance with the sequence. Although this method can solve the above-described problems, a large buffer memory is required, and processing is complex.

[0022]

As the third problem, when a binarization error is to be distributed to neighboring pixels, a

product-sum operation is necessary, and the calculation amount is large. To solve this problem, Japanese Patent Laid-Open Nos. 64-18369 and 1-284172 disclose binarization schemes which use a value such as 1/2, 1/4, or 1/8, which is easy to calculate, as a weight coefficient in binarization error distribution. These schemes facilitate calculation as compared to the prior art but are still complex as compared to the dither method.

[0023]

As the fourth problem, a buffer memory having a large storage capacity is necessary for storing binarization errors. The dither method requires no buffer memory. However, the error diffusion method can obtain a higher image quality. The delta-sigma modulation is a binarization scheme which executes processing similar to that of the error diffusion method without requiring any large buffer memory. However, this scheme cannot obtain a high image quality.

[0024]

As the fifth problem, when a binary image signal obtained by the error diffusion method is to be encoded using MH encoding or MR encoding, information compression is difficult, and the information amount sometimes increases if anything. This is because MH encoding or MR encoding is an encoding scheme that is

based on the concentration of white pixels or black pixels in a binary image signal. A binary image signal obtained by the error diffusion method expresses the halftone of the density. Since white pixels and black pixels are scattered like a stipple pattern. Hence, when such an encoding scheme is used, the encoding efficiency becomes low. To solve this problem, Japanese Patent Laid-Open No. 2-182080 discloses a binarization scheme which feeds back a binarization result to a comparator to impart a hysteresis characteristic to a binarizer. In this scheme, pixels having the same value are continuously laid out in the main scanning or sub scanning direction. In addition, the error diffusion method is used simultaneously. Hence, the binary image signal preserves the gray level. This scheme can generate a binary image signal that has a good affinity to MH encoding or MR encoding. However, the relationship between the hysteresis characteristic of the binarizer and the error diffusion method has not been examined at all. Also, this scheme is not designed to freely control the characteristic of the obtained binary image signal. Furthermore, the obtained binary image signal contains a number of short discrete runs, and therefore, the image quality is poor.

[0025]

The present invention has been made to solve the

above-described problems, and has as its object to provide an image signal processing system which uses a buffer memory or similar memory having a relatively small storage capacity and obtains a binary image signal of a high-quality pseudo halftone image with a simple arrangement.

[0026]

[Means of Solving the Problems]

In order to achieve the above object, according to the present invention, an image signal processing system for converting halftone image information into a binary image signal by using an error diffusion scheme comprises first means comprising binarization means for binarizing halftone image information of each pixel, error generation means for obtaining an error in the binarization, storage means for storing upper bits of the binarization error obtained by the error generation means, latch means for latching lower bits of the binarization error, and feedback means for feeding back outputs from the storage means and the latch means to an input of the binarization means.

[0027]

In order to achieve the above object, according to the present invention, an image signal processing system for converting halftone image information into a binary image signal by using an error diffusion scheme comprises second means comprising binarization means

for parallelly binarizing pieces of halftone image information of a plurality of pixels that are adjacent to each other, a plurality of error generation means for obtaining errors in the binarization of the respective pixels, average value means for averaging the binarization errors from the plurality of error generation means, storage means for storing the averaged binarization error, and feedback means for feeding back an output from the storage means to each input of the binarization means.

[0028]

In order to achieve the above object, according to the present invention, an image signal processing system for converting halftone image information into a binary image signal by using an error diffusion scheme comprises third means comprising binarization means for binarizing halftone image information of each pixel, error generation means for obtaining an error in the binarization, storage means for storing the binarization error obtained by the error generation means, and feedback means for feeding back an output from the storage means to the binarization means through an error distributor, wherein when binarization errors obtained from neighboring pixels around halftone image information derived from a pixel of interest are to be distributed, the error distributor expresses each of the binarization errors generated from the

neighboring pixels by a binary number, assigns a specific bit of the binary number to each of the neighboring pixels in accordance with a position of the neighboring pixel, and adds the assigned bits to define a distribution amount.

[0029]

In order to achieve the above object, according to the present invention, an image signal processing system for converting halftone image information into a binary image signal by using an error diffusion scheme comprises fourth means comprising binarization means for binarizing halftone image information of each pixel, error generation means for obtaining an error in the binarization, latch means for latching the binarization error obtained by the error generation means, feedback means for feeding back an output from the latch means to the binarization means, and correction means for increasing a halftone reproducibility in a sub scanning direction.

[0030]

[Operation of the Invention]

According to the first means, the storage means for storing the upper bits of the binarization error and the latch means for latching the lower bits of the binarization error are arranged so that the function of the conventional buffer memory is distributed to the storage means and the latch means. For this reason,

the storage capacity of the storage means serving as a buffer memory can be reduced.

[0031]

According to the second means, the errors in the binarization of the plurality of pixels are averaged. The averaged binarization error is stored in the storage means, i.e., a buffer memory. Hence, the storage capacity of the storage means can be reduced as compared to an arrangement that causes a buffer memory to individually store binarization errors from a plurality of pixels.

[0032]

According to the third means, to calculate the distribution ratio of errors to be added to pixels at the output of a buffer memory serving as the storage means, an error distributor in which the distribution ratio is set as a hardware structure is used. For this reason, the calculation to distribute the binarization errors is very simple.

[0033]

According to the fourth means, only the latch means for latching the binarization error is used, and no buffer memory is used. For this reason, the storage capacity of the storage device can be largely reduced. In addition, the means for correcting the halftone reproducibility in the sub scanning direction is arranged. Hence, the degradation in halftone

reproducibility in the sub scanning direction due to the binary image signal can be minimized.

[0034]

[Embodiments]

The embodiments of the present invention will be described below with reference to the accompanying drawings.

[0035]

Fig. 1 is a block diagram showing an image signal processing apparatus according to the first embodiment of the present invention.

[0036]

Referring to Fig. 1, reference numeral 1 denotes a binarizer; 2, an adder; 3, a buffer memory; 4, a latch circuit; 5, an error filter; and 6, an adder.

[0037]

The upper bits of a binarization error obtained from the adder 2 are supplied to the buffer memory 3. The remaining lower bits of the binarization error are supplied to the latch circuit 4.

[0038]

In this arrangement, halftone image information input from a pixel to be binarized is supplied to the adder 6 and added to the output from the error filter 5. The added halftone image information is then supplied to the binarizer 1 and converted into a binary image signal by binarization. The adder 2 subtracts

the binary image signal from the added halftone image information to generate a binarization error. The obtained binarization error is divided into upper and lower portions of appropriate bits. The upper bits are stored in the buffer memory 3. The remaining lower bits are subjected to sign extension and then stored in the latch circuit 4. The sum of values stored in the buffer memory 3 and latch circuit 4 is equal to the value of the original binarization error, as a matter of course. The upper bits of the binarization error, which are stored in the buffer memory 3, are distributed to a plurality of pixels, as in the conventional error diffusion method. On the other hand, the lower bits of the binarization error, which are stored in the latch circuit 4, are added to halftone image information subsequently input to the adder 6.

[0039]

According to this embodiment, the bus width of the buffer memory 3 only needs to be equal to the number of bits (the number can arbitrarily be set) of the upper portion. Hence, the buffer memory 3 has a bit width smaller than that of a conventional buffer memory. The bit width can arbitrarily be set. For example, even when halftone image information to be binarized contains 6 bits and 64 gray levels, the buffer memory 3 can use a 4-bit width. For this

reason, the storage capacity of the buffer memory 3 can be reduced. In addition, the degree of freedom in designing the error diffusion circuit increases.

[0040]

Fig. 2 is a block diagram showing an image signal processing apparatus according to the second embodiment of the present invention.

[0041]

Referring to Fig. 2, reference numeral 7 denotes a binarizer; 8 and 9, adders; 10, an averaging circuit; 11, a buffer memory; 12, an error filter; and 13 and 14, adders.

[0042]

The binarizer parallelly binarizes separate pieces of halftone image information which are supplied from two inputs and outputs separate binary image signals. In this embodiment, pieces of halftone image information obtained from two adjacent pixels are binarized together. The two pieces of halftone image information obtained from the two pixels are supplied to the adders 13 and 14 and added to outputs from the error filter 5, respectively. The two pieces of added halftone image information are supplied to the binarizer 7 and parallelly converted into two binary image signals by binarization. At this time, the adders 8 and 9 separately subtract the binary image signals from the added halftone image information to

generate binarization errors. The two obtained binarization errors are supplied to the averaging circuit 10. The averaging circuit 10 calculates the average value of the binarization errors. The calculated value is stored in the buffer memory 11 as the representative value of the binarization errors generated in the two pixels. The binarization error stored in the buffer memory 11 is read out, as needed, weighted by the error filter 12, and added to pieces of halftone image information subsequently input to the adders 13 and 14.

[0043]

According to this embodiment, instead of directly storing the binarization errors obtained by the adders 8 and 9, a representative value is obtained for every two pixels and stored. For this reason, the size of the buffer memory 11 can be about halved from the prior art. In addition, the frequency of the read and write accesses to the buffer memory 11 also decreases. Hence, the memory access time is relaxed, and high-speed processing can be executed. Furthermore, calculation to distribute the value read out from the buffer memory 11 to halftone image information can also be simplified.

[0044]

In this embodiment, binarization is performed for every two pixels, and binarization errors are averaged.

However, the processing need not always be executed for every two pixels. The processing may be executed for every arbitrary number n of pixels (n is two or more).

[0045]

Fig. 3 is a block diagram showing an image signal processing apparatus according to the third embodiment of the present invention.

[0046]

The same reference numerals as in Figs. 1 and 2 denote the same constituent elements in Fig. 3.

[0047]

The third embodiment is a combination of the first and second embodiments. As in the second embodiment, pieces of halftone image information obtained from two adjacent pixels are binarized together. The values of pieces of halftone image information obtained from the two pixels are corrected by adders 13 and 14, respectively. The corrected values are supplied to a binarizer 7 and parallelly converted into two binary image signals by binarization. Adders 8 and 9 separately generate binarization errors. The two binarization errors are averaged by an averaging circuit 10 so that an averaged binarization error is obtained. The averaged binarization error is divided into upper bits and remaining lower bits. Only the upper bits are stored in a buffer memory 3. The lower bits are subjected to

sign compensation and then stored in a latch circuit 4. A value obtained by doubling the sum of values stored in the buffer memory 3 and latch circuit 4 is equal to the sum of the values of the two original binarization errors.

[0048]

Subsequently, the lower bits of the binarization error, which are stored in the latch circuit 4, are read out for binarization processing of the next pixel and sent to the adders 13 and 14 through an error filter 12. The read is executed in the following way. The lower bits of the binarization error, which are stored in the latch circuit 4, are read out and sent to the error filter 12 when halftone image information obtained from the immediately succeeding pixel is input. The upper bits of the binarization error, which are stored in the buffer memory 3, are repeatedly read out and sent to the error filter when halftone image information from a pixel that exists in the error distribution range. That is, the upper bits of the binarization error, which are stored in the buffer memory 3, are stored for a while and distributed to a plurality of pixels. On the other hand, the lower bits of the binarization error, which are stored in the latch circuit 4, are distributed to only the next pixel.

[0049]

This embodiment has both the advantages of the first and second embodiments.

[0050]

Fig. 4 is a block diagram showing an image signal processing apparatus according to the fourth embodiment of the present invention.

[0051]

Referring to Fig. 4, reference numeral 15 denotes a converter; 16 and 18, inverse converters; and 17, an adder. The same reference numerals as in Fig. 1 denote the same constituent elements in Fig. 4.

[0052]

The converter 15 executes bit compression. The inverse converters 16 and 18 execute bit expansion.

[0053]

In this embodiment, a binarization error obtained by an adder 2 is replaced with a representative value by appropriate conversion by the converter 15 and then stored in a buffer memory 3. The number of bits to be used to express the representative value is smaller than the number of bits of the original binarization error. The binarization error expressed by the smaller number of bits and stored in the buffer memory 3 is read out from the buffer memory 3, and returned by the inverse converter 18 to the binarization error expressed by the original number of bits and sent to an error filter 5. The value of the binarization error

whose number of bits is decreased once does not coincide with the value of the binarization error expressed by the original number of bits even after inverse conversion. A correction value is written in a latch circuit 4 to adjust the value of the binarization error. The correction value corresponds to the difference between the value of the binarization error before conversion by the converter 15 and the value of the original binarization error obtained by the inverse converter 16. The two inverse converters 16 and 18 have the same characteristic.

[0054]

Various types of converters can be used as the converter 15. When a converter that discards the lower bits is used as the converter 15, the processing is substantially the same as in the first embodiment. When a one- or two-dimensional low-pass filter 19 and a down-sampling circuit 20 which thins out pixel by pixel are combined, as shown in Fig. 5(a), the processing is substantially the same as in the second or third embodiment. In this case, the buffer memory 3 which stores the representative value needs to store only the binarization error value every other pixel. Hence, the storage capacity can be further decreased. When the device shown in Fig. 5(a) is used as the converter 15, a combination of an interpolation circuit 21 which executes bit interpolation and a one- or

two-dimensional low-pass filter 22, as shown in Fig. 5(b), is preferably used as the inverse converters 16 and 18.

[0055]

Fig. 6 is a block diagram showing an image signal processing apparatus according to the fifth embodiment of the present invention.

[0056]

Referring to Fig. 5, reference numeral 23 denotes an adder; and 24, a bias generation circuit. The same reference numerals as in Fig. 1 denote the same constituent elements in Fig. 6.

[0057]

The AC bias generation circuit 24 generates, e.g., a bias voltage having the same magnitude and a polarity that is inverted for each line.

[0058]

In this embodiment, a binarization error is supplied to a latch circuit 4 to store all the bits of the binarization error. According to this arrangement, a buffer memory 3 can be omitted so that the scale of the error diffusion circuit can greatly be reduced. However, this circuit is equivalent to that of the conventionally known delta-sigma modulation scheme. All the bits of the binarization error are distributed in the main scanning direction. For this reason, the quality of an image obtained by binarization in the

above arrangement degrades so that, e.g., a vertical stripe pattern is formed. This phenomenon occurs because the binarization error is distributed only in the main scanning direction, and the halftone reproducibility in the sub scanning direction cannot be maintained. To solve this problem, the present invention improves the halftone reproducibility in the sub scanning direction by using a correction circuit.

[0059]

In this embodiment, the correction circuit is constituted by the adder 23 and AC bias generation circuit 24. Halftone image information obtained from a pixel is added first by the adder 23 to the output from the bias generation circuit 24. The bias generation circuit 24 generates an output voltage corresponding to a positive constant +c or a negative constant -c. The output polarity changes every time the binarization processing progresses by one line in the sub scanning direction. The output from the adder 23 is corrected by an adder 6 in association with the binarization error and binarized by a binarizer 1. An adder 2 generates a binarization error. The binarization error is stored in the latch circuit 4. The binarization error stored in the latch circuit 4 is sent to an error filter 5 and used to correct subsequently input halftone image information. The error filter 5 is formed from a one-dimensional low-pass filter.

[0060]

In this embodiment, the halftone reproducibility in the sub scanning direction is increased by applying an AC bias in the sub scanning direction. Since the buffer memory 3 can be omitted, the circuit scale is small. Employment of the bias generation circuit 24 is easier than a dither matrix used in the conventional dither method. A binary image obtained in this embodiment has an intermediate nature between a binary image obtained by a conventional error diffusion circuit and that obtained by the dither method. The code amount in MH or MR encoding also has an intermediate value between them.

[0061]

Fig. 7 is a block diagram showing an image signal processing apparatus according to the sixth embodiment of the present invention.

[0062]

Referring to Fig. 7, reference numeral 25 denotes a binary buffer memory; 26, a two-dimensional low-pass filter; and 27, an adder. The same reference numerals as in Fig. 1 denote the same constituent elements in Fig. 7.

[0063]

A feedback circuit formed from the binary buffer memory 25, two-dimensional low-pass filter 26, and adder 27 constitutes a correction circuit.

[0064]

Halftone image information obtained from a pixel is first added by the adder 27 to the output from the two-dimensional low-pass filter 26, corrected by an adder 6 in association with the binarization error, and binarized by a binarizer 1. The binarized binary image signal is stored in the binary buffer memory 25 and then input to the two-dimensional low-pass filter 26. An adder 2 calculates a binarization error. The binarization error is stored in a latch circuit 4. The binarization error read out from the latch circuit 4 is sent to an error filter 5 and used to correct subsequently input image signal processing apparatus.

[0065]

According to this embodiment, when the binary image signal is fed back, the low-frequency component of the binarization error in the sub scanning direction is attenuated, and the high-frequency component is enhanced. When the low-frequency component of the binarization error is attenuated, the gray level storage property is improved. As a side effect, the high-frequency component of the resultant binary image itself is also enhanced. However, high-frequency enhancement processing is often executed for edge enhancement or the like as pre-processing of binarization. Hence, this side effect can be positively utilized.

[0066]

In this case, the binary buffer memory 25 used in this embodiment stores a binary image with 1 bit for one pixel. Hence, the binary buffer memory 25 can have a smaller capacity than a buffer memory 3 which stores binarization errors. To encode the resultant binary image, a buffer memory which stores the binary image is required in many cases, as in, e.g., MR encoding used in a facsimile apparatus. In this embodiment, the binary buffer memory 25 can also be used for this purpose so that the circuit scale can be reduced.

[0067]

Fig. 8 is a block diagram showing an image signal processing apparatus according to the seventh embodiment of the present invention.

[0068]

Referring to Fig. 8, reference numeral 28 denotes an error distributor. The same reference numerals as in Fig. 1 denote the same constituent elements in Fig. 8. Fig. 9 is a view showing a detailed structure of the error distributor 28.

[0069]

A halftone image signal obtained from a pixel is added by an adder 6 to the output from the error distributor 28 and binarized by a binarizer 1. At this time, the threshold value of the comparator of the binarizer 1 is defined such that a binarization error

always has a positive value or zero. A binarization error is obtained by an adder 2 and stored in a buffer memory 3. The error distributor 28 calculates a value to be used to correct subsequently input halftone image information on the basis of the value of the binarization error read out from the adder 6. This calculation is performed not by calculating a weighted mean but by combining bit lines.

[0070]

As shown in Fig. 9, the error distributor 28 assigns a specific bit of a binary number to each of pixels laid out around a pixel of interest. For example, the least significant bit "1" is assigned to a pixel a. An intermediate bit "4" is assigned to a pixel b. An intermediate bit "2" is assigned to a pixel c. The most significant bit "8" is assigned to a pixel d. That is, binarization errors generated from four pixels near the pixel to be binarized in the halftone image information are extracted from the buffer memory 3. Each of signal lines 8a, 8b, 8c, and 8d that represent the binarization errors read out from the buffer memory 3 corresponds to a binarization error generated from one pixel. The signal lines 8a, 8b, 8c, and 8d are 4-bit signal lines and are weighted by 1, 2, 4, and 8, respectively. Hence, the binarization errors always have nonnegative values. The bit lines will be represented by a1, a2, a4, a8, b1, b2,.... hereinafter.

[0071]

Assume that the signal lines a1, b4, c2, and d8 of 16 signal lines a1 to d8 are input to the adder 6 in accordance with the above-described assignment. Values added to the halftone image information by the adder 6 are a1 × 1 + b4 × 4 + c2 × 2 + d8 × 8. The binarization errors are decomposed for each bit line. Since all the binarization errors are finally distributed to the neighboring pixels, the gray level storage property is maintained.

[0072]

According to this embodiment, calculation for distributing the binarization errors to the neighboring pixels is unnecessary. Hence, the circuit structure is very simple.

[0073]

Some examples of the structure of the binarizer used in the above-described embodiments will be described next.

[0074]

Fig. 10 is a view showing an example of a binarization circuit used as the binarizer 7 of the second and third embodiments.

[0075]

Referring to Fig. 10, reference numeral 29 denotes an adder; 30, 31, and 32, comparators; and 33, a selector.

[0076]

In the operation of this example, two pieces of input halftone image information x1 and x2 are sent to the adder 29 to obtain a sum s. The sum s is compared with each of threshold values s1 and s2 by the comparators 30 and 31. As a result, binary outputs y1 and y2 below are obtained.

[0077]

①. When $s < s1$, the binary outputs satisfy $y1 = y2 = 0$. ②. When $s > s2$, the binary outputs satisfy $y1 = y2 = 1$. ③. When $s1 \leqq s \leqq s2$, and $x1 \leqq x2$, $y1 = 0$ and $y2 = 1$. When $x1 > x2$, $y1 = 1$ and $y2 = 0$. In this case, y1 and y2 are binary image signals corresponding to the two pieces of halftone image information x1 and x2.

[0078]

When this binarization circuit is independently used, binarization is executed in consideration of the values of two pixels. Hence, even through the arrangement is simple, the gray level can be maintained to some extent. When this binarization circuit is applied to the binarizer 7 of the second embodiment, the phenomenon that even when the values of two adjacent pixels a and b have a relationship $a > b$, 0 is assigned to the pixel a while 1 is assigned to the pixel b hardly takes place because the relationship between the two pixels is taken into consideration.

Hence, a binary image signal with a clear edge portion can be obtained.

[0079]

Fig. 11 is a view showing the first example of a binarization circuit used as the binarizer 1 of the first and second embodiments.

[0080]

Referring to Fig. 11, reference numerals 34 and 35 denote comparators; 36, a selector; and 37, a delay device for one pixel.

[0081]

In the operation of this example, an input halftone image signal x is compared with two threshold values s1 and s2 by the comparators 34 and 35. As a comparison result, a binary output y below is obtained.

[0082]

①. When $x \leqq s1$, $y = 0$. ②. When $x \geqq s2$, $y = 1$. ③. When $s1 < x < s2$, y is an immediately preceding output value.

[0083]

The binary image signal obtained by this binarization circuit is suitable for MH encoding because runs in the horizontal direction readily continue. In addition, since no feedback to the comparator is present, the processing speed can easily be increased by employing pipeline processing.

[0084]

Fig. 12 is a view showing the second example of the binarization circuit used as the binarizer 1 of the first and second embodiments.

[0085]

Referring to Fig. 12, reference numeral 38 denotes a delay device for one line. The same reference numerals as in Fig. 11 denote the same constituent elements in Fig. 12.

[0086]

In this example, the delay device 38 for one line is used in place of the delay device 37 for one pixel in the first example. The input halftone image signal x is compared with the two threshold values s1 and s2 by the comparators 34 and 35, respectively. As a comparison result, the binary output y below is obtained.

[0087]

①. When $x \leqq s1$, $y = 0$. ②. When $x \geqq s2$, $y = 1$. ③. When $s1 < x < s2$, y is a value output for an immediately preceding line, which is stored in the delay device 38 for one line, which serves as a buffer memory.

[0088]

The binary image signal obtained by this binarization circuit is suitable for MR encoding because runs in the vertical direction readily continue. In addition, since no feedback to the

comparator is present, the processing speed can easily be increased by employing pipeline processing.

[0089]

Fig. 13 is a view showing the third example of the binarization circuit used as the binarizer 1 of the first and second embodiments.

[0090]

Referring to Fig. 13, reference numeral 39 denotes an inverter. The same reference numerals as in Fig. 11 denote the same constituent elements in Fig. 13.

[0091]

In this example, the inverter 39 is arranged next to the delay device 37 for one pixel in the first example. The input halftone image signal x is compared with the two threshold values s1 and s2 by the comparators 34 and 35. As a comparison result, the binary output y below is obtained.

[0092]

①. When $x \leqq s1$, $y = 0$. ②. When $x \geqq s2$, $y = 1$. ③. When $s1 < x < s2$, y is a value opposite to the immediately preceding output value.

[0093]

The binary image signal obtained by this binarization circuit is suitably used to binarize the halftone image information because white pixels and black pixels are scattered.

[0094]

Fig. 14 is a view showing the fourth example of the binarization circuit used as the binarizer 1 of the first and second embodiments.

[0095]

The same reference numerals as in Fig. 13 denote the same constituent elements in Fig. 14.

[0096]

In this example, the inverter 39 is arranged next to the delay device 38 for one line in the second example. The halftone image signal x is compared with the two threshold values s1 and s2 by the comparators 34 and 35. As a comparison result, the binary output y below is obtained.

[0097]

①. When $x \leqq s1$, $y = 0$. ②. When $x \geqq s2$, $y = 1$. ③. When $s1 < x < s2$, y is a value opposite to the value output for an immediately preceding line, which is stored in the delay device 38.

[0098]

The binary image signal obtained by this binarization circuit is suitably used to binarize the halftone image information because white pixels and black pixels are scattered. This binarization circuit improves the halftone image reproducibility in the vertical direction. Hence, when the binarization circuit is applied to the error diffusion circuit shown

in Fig. 6 or 7, a large effect can be obtained. Especially, when the binarization circuit is applied to the error diffusion circuit shown in Fig. 7, which enhances the high-frequency component of the screen, various image qualities can be obtained.

[0099]

The binarization circuits of the first to fourth examples may be combined. When the length of delay of the delay device 38 for one line is changed, runs can be tilted in a direction other than the horizontal and vertical directions.

[0100]

Generally, oblique runs have a small visual effect on the image quality as compared to horizontal or vertical runs. In MR encoding, encoding is performed by using correlation in the vertical direction. Even for oblique runs, if the tilt is almost vertical, the encoding efficiency increases. However, in the MR encoding, when a pass mode is generated, the code amount increases. Hence, the manner the tilt of runs is applied must be carefully set.

[0101]

Fig. 15 is a view showing the fifth example of the binarization circuit used as the binarizer 1 of the first and second embodiments.

[0102]

Referring to Fig. 15, reference numerals 40, 41, and 42 denote comparators; 43, a selector; 44, a delay device for one line; 45, a delay device for one pixel; 46, an OR gate; and 47, an AND gate.

[0103]

In this example, the AND and OR between the binarization result of an immediately preceding pixel and that of an immediately preceding line are used as predicted values. The input halftone image signal x is compared with three threshold values s1, s2, and s3 by the comparators 40, 41, and 42, respectively. As a comparison result, the binary output y below is obtained.

[0104]

①. When $x \leqq s1$, $y = 0$. ②. When $s1 < x \leqq s2$, y is the value of the AND between the binarization result of an immediately preceding pixel and that of an immediately preceding line. ③. When $s2 < x \leqq s3$, y is the value of the OR between the binarization result of the immediately preceding pixel and that of the immediately preceding line. ④. When $s3 < x$, $y = 1$.

[0105]

The binary image signal obtained from this binarization circuit is suitable for MR encoding because white pixels and black pixels readily concentrate. In addition, since no feedback to the comparators 40 to 42 is present, the processing speed

can easily be increased by employing pipeline processing.

[0106]

The binarization circuit of this example logically calculates the values of adjacent pixels, which are already binarized, to prepare a plurality of predicted values. A binarization scheme which prepares a plurality of predicted values by another method and selects an appropriate predicted value in accordance with the value of the input halftone image information x may be used.

[0107]

Fig. 16 is a view showing the sixth example of the binarization circuit used as the binarizer 1 of the first and second embodiments.

[0108]

Referring to Fig. 16, reference numeral 48 denotes a binary buffer memory; and 49, a predictor. The same reference numerals as in the first example denote the same constituent elements in Fig. 16.

[0109]

In this example, the delay device 37 for one pixel or the delay device 38 for one line shown in the above examples is replaced with the binary buffer memory 48 and predictor 49. When the first to fifth examples are totally combined, the arrangement of this example can be obtained.

[0110]

In the operation of this example, the input halftone image signal x is compared with the two threshold values s1 and s2 by the comparators 34 and 35. The values of already binarized pixels near the signal x are stored in the binary buffer memory 48. The predictor 49 predicts a predicted value y' of the binarization result of the signal x from the contents of the binary buffer memory 48. The predicted value y' is also a binary value, i.e., 0 or 1. As a comparison result by the comparators 34 and 35, the binary output y below is obtained.

[0111]

①. When $x \leqq s1$, $y = 0$. ②. When $s1 < x \leqq s2$, $y = y'$. ③. When $s2 < x$, $y = 1$.

[0112]

The binarization circuit of this example outputs 0 or 1 when the signal x to be binarized is close to 0 or 1 ($x \leqq s1$ or $s2 < x$). When the signal x is apart from 0 or 1, the binarization circuit outputs the predicted value y'. More specifically, the predicted value y' is output when the error is large independently of whether 0 or 1 is output. If the error is large independently of the output value, a value more convenient for prediction is output. The binary output y may coincide with the predicted value y' in some cases even when the signal x is close to 0

or 1.

[0113]

When the binary image signal obtained by the binarization circuit of this example should be encoded, not the binary image signal itself but information representing whether the predicted value y' by the predictor 49 coincides with the binary output y is encoded. This decreases the code amount. The predictor is also required for decoding a binary image signal. The predictor to be used for encoding and decoding must be operated using the same initial value. When a binary image signal is transmitted as an encoded signal by this scheme, the code amount can be reduced.

[0114]

Fig. 17 is a view showing the second example of the binarization circuit used as the binarizer 7 of the second and third embodiments.

[0115]

Referring to Fig. 17, reference numerals 50 and 51 denote comparators; 52 and 53, adders; and 54, a multiplier.

[0116]

In this example, the two pieces of input halftone image information x1 and x2 are binarized in the following way. First, the information x1 is compared with the threshold value s1 by the comparator 50 and binarized. A binarization error generated at this time

is obtained by the adder 52. The binarization error is appropriately weighted by the multiplier 54. The adder 53 corrects the information x2. The corrected information x2 is binarized by the comparator 51.

[0117]

When the binarization circuit of this example is independently used, the binarization error generated in the first pixel is canceled in the second pixel. Hence, the gray level is preserved to some extent. When the binarization circuit of this example is applied to the binarizer 7 of the error diffusion circuit shown in Fig. 2, an error diffusion circuit which executes binarization for each pixel, like the conventional error diffusion circuit, is constituted.

[0118]

An encoding circuit used in the image signal processing system of the present invention will be described next.

[0119]

Fig. 18 is a block diagram showing the first example of the encoding circuit.

[0120]

Referring to Fig. 18, reference numeral 55 denotes an MR encoder. The same reference numerals as in Fig. 7 denote the same constituent elements in Fig. 18.

[0121]

In this example, the MR encoder 55 is added to the error diffusion circuit shown in Fig. 7 to form an encoding circuit. In the MR encoder 55, binary data of one line, which is stored in the binary buffer memory 25, is received by the reference line. In addition, binary image signal data obtained at the output of the binarizer 1 is received by the encoding line. MR encoding is thus executed.

[0122]

In this example, the binary buffer memory 25 in the correction circuit of the error diffusion circuit is also used as the line memory necessary in MR encoding. Accordingly, the total storage capacity of the storage device can be reduced.

[0123]

Fig. 19 is a block diagram showing the second example of the encoding circuit.

[0124]

Referring to Fig. 19, reference numeral 56 denotes an MR encoder. The same reference numerals as in Fig. 16 denote the same constituent elements in Fig. 19.

[0125]

In this example, the MR encoder 56 is added to the binarization circuit shown in Fig. 16 to form an encoding circuit. In the MR encoder 56, binary data of one line, which is stored in the binary buffer memory

48, is received by the reference line. In addition, binary image signal data obtained at the output of the selector 36 is received by the encoding line. MR encoding is thus executed.

[0126]

In this example as well, the binary buffer memory 48 in the binarization circuit is also used as the line memory necessary in MR encoding. Accordingly, the total storage capacity of the storage device can be reduced.

[0127]

Fig. 20 is a block diagram showing an example of an encoding circuit which encodes information representing the coincidence between the predicted value of the predictor and the value of a binary image signal obtained by the binarization circuit shown in Fig. 16.

[0128]

Referring to Fig. 20, reference numeral 57 denotes a comparator; and 58, a binary signal encoder. The same reference numerals as in Fig. 16 denote the same constituent elements in Fig. 20.

[0129]

In this example, the comparator 57 and binary signal encoder 58 are added to the binarization circuit shown in Fig. 16 to encode binary information representing the coincidence between the predicted

value y' of the predictor 49 and the value y of a binary image signal obtained at the output of the selector 36. The comparator 57 compares the predicted value y' with the value y of the binary image signal and outputs the comparison result as binary information 0 (coincidence) or 1 (non-coincidence). The binary signal encoder 58 generates an encoding output by encoding the binary information.

[0130]

In this example, encoded information is transmitted in correspondence with information 0 or 1. Hence, information can be compressed in accordance with the number of times of appearance of 0 and 1.

[0131]

Fig. 21 is a block diagram showing an example of a decoding circuit which decodes information that is encoded by the encoding circuit shown in Fig. 20.

[0132]

Referring to Fig. 21, reference numeral 59 denotes a binary information decoder; 60, a selector; 61, a binary buffer memory; and 62, a predictor.

[0133]

In the operation of this example, binarization information supplied from the encoding circuit shown in Fig. 20 is received by the binary information decoder 59 first and decoded to information 0 or 1. The decoded information is supplied to the selector 60.

The selector 60 is controlled by the predicted value of the predictor 62 that is the same as the predictor 49 used in encoding circuit shown in Fig. 20. In this control, when the decoded information is 0, it coincides with the output from the predictor 62. Hence, the selector 60 generates the output of the predictor 62. When the decoded information is 1, it does not coincide with the output from the predictor 62. Hence, the selector 60 generates the inverted output of the predictor 62.

[0134]

When the encoding circuit shown in Fig. 20 and the decoding circuit of this example are used together, the predictors 49 and 62 must have the same characteristics, as described above. In addition, the binary buffer memories 48 and 61 must have the same initial state (all bits are 0 or 1). In this arrangement, values output from the predictors 49 and 62 always coincide with each other. The encoding circuit shown in Fig. 20 encodes and transmits only resultant information 0 or 1, which represents coincidence or non-coincidence. In this case, the same binary image signal as that output from the encoding circuit shown in Fig. 20 can be obtained at the output of the decoding circuit of this example.

[0135]

When the encoding circuit and decoding circuit

are used together, the value of the binary image signal and the predicted value normally coincide with each other. Hence, the binarization information is often 0 (coincidence). When the binary signal encoder 58 and binarization information decoder suitable for this bias are used, the information amount to be transmitted can be reduced.

[0136]

[Effects of the Invention]

According to the present invention, as the first effect, in the binarization error stored in the buffer memory 3, the number of bits to be stored is decreased, or an average value for a plurality of pixels is stored. For this reason, the storage capacity of the buffer memory 3 can be reduced, and the size can be made small. When the storage capacity of the buffer memory 3 decreases, the number of times of information write/read in/from the buffer memory 3 can also be reduced. Hence, the processing speed that has been limited by the memory access time can be increased.

[0137]

As the second effect, when the average value of binarization errors is calculated in advance and then stored in the buffer memory 3, the calculation amount of weighting by the error filter 12 can be reduced.

[0138]

As the third effect, when the system for

combining bit lines is employed as the arithmetic means of the error filter 5 that distributes binarization errors, arithmetic processing for distributing the errors is greatly simplified.

[0139]

As the fourth effect, when a plurality of pixels are to be simultaneously binarized, the binarization can be performed in consideration of the relationship between adjacent pixels. For this reason, a high image quality can be obtained. In addition, errors are distributed in blocks of a plurality of pixels. Hence, error distribution corresponding to the state of each adjacent pixel can be taken into consideration so that a high image quality can be obtained.

[0140]

Furthermore, the binarization circuit used in the present invention can have a hysteresis characteristic, although it executes no feedback to a comparator. The binarization circuit is suitable for increasing the processing speed by employing pipeline processing. When the binarization circuit is applied to an error diffusion circuit, distribution of white pixels and black pixels can be controlled. Hence, when a specific encoding scheme is selected, a binary image signal for a high encoding efficiency can be generated while avoiding any degradation in image quality.

[Brief Description of the Drawings]

[Fig. 1]

Fig. 1 is a block diagram showing an image signal processing apparatus according to the first embodiment of the present invention.

[Fig. 2]

Fig. 2 is a block diagram showing an image signal processing apparatus according to the second embodiment of the present invention.

[Fig. 3]

Fig. 3 is a block diagram showing an image signal processing apparatus according to the third embodiment of the present invention.

[Fig. 4]

Fig. 4 is a block diagram showing an image signal processing apparatus according to the fourth embodiment of the present invention.

[Figs. 5(a) and 5(b)]

Figs. 5(a) and 5(b) are block diagrams showing examples of a converter and an inverse converter used in the fourth embodiment.

[Fig. 6]

Fig. 6 is a block diagram showing an image signal processing apparatus according to the fifth embodiment of the present invention.

[Fig. 7]

Fig. 7 is a block diagram showing an image signal processing apparatus according to the sixth embodiment

of the present invention.

[Fig. 8]

Fig. 8 is a block diagram showing an image signal processing apparatus according to the seventh embodiment of the present invention.

[Fig. 9]

Fig. 9 is a view showing a detailed structure of an error distributor.

[Fig. 10]

Fig. 10 is a view showing an example of a binarization circuit used as a first binarizer.

[Fig. 11]

Fig. 11 is a view showing the first example of a binarization circuit used as a second binarizer.

[Fig. 12]

Fig. 12 is a view showing the second example of the binarization circuit used as the second binarizer.

[Fig. 13]

Fig. 13 is a view showing the third example of the binarization circuit used as the second binarizer.

[Fig. 14]

Fig. 14 is a view showing the fourth example of the binarization circuit used as the second binarizer.

[Fig. 15]

Fig. 15 is a view showing the fifth example of the binarization circuit used as the second binarizer.

[Fig. 16]

Fig. 16 is a view showing a combined example of the first to fifth examples of the binarization circuit used as the second binarizer.

[Fig. 17]

Fig. 17 is a view showing an example of a binarization circuit which simultaneously binarizes two pixels.

[Fig. 18]

Fig. 18 is a block diagram showing the first example of an encoding circuit.

[Fig. 19]

Fig. 19 is a block diagram showing the second example of the encoding circuit.

[Fig. 20]

Fig. 20 is a block diagram showing the third example of the encoding circuit.

[Fig. 21]

Fig. 21 is a block diagram showing an example of a decoding circuit.

[Figs. 22(a) and 22(b)]

Figs. 22(a) and 22(b) are block diagram showing a known delta-sigma modulation circuit.

[Fig. 23]

Fig. 23 is a block diagram showing an example of a binarization circuit by a conventional error diffusion method.

[Fig. 24]

Fig. 24 is a view showing a state wherein errors from

neighboring pixels are distributed in the error diffusion method.

[Description of the Reference Numerals]

1, 7	binarizer
2, 6, 8, 9, 13, 14, 17, 23, 27, 29, 52, 53	adder
3, 11, 25, 48, 61	buffer memory
4	latch circuit
5, 12	error filter
10	averaging circuit
15	converter
16, 18	inverse converter
19, 22	one- or two-dimensional low-pass filter
20	down-sampling circuit
21	interpolation circuit
24	bias generator
26	two-dimensional low-pass filter
28	error distributor
30, 31, 32, 34, 35, 40, 41, 42, 50, 51, 57	comparator
33, 36, 43, 60	selector
37, 45	delay device for one pixel
38, 44	delay device for one line
39	inverter
46	OR gate
47	AND gate

49, 62	predictor
54	multiplier
55, 56	MR encoder
58	binary information encoder
59	binary information decoder

FIG. 1

(1): HALFTONE IMAGE

(2): BINARY IMAGE

(3): LOWER BITS AND SIGN OF BINARIZATION ERROR

(4): UPPER BITS OF BINARIZATION ERROR

1: BINARIZER

3: BUFFER MEMORY

4: LATCH

5: ERROR FILTER

FIG. 2

(1): BINARIZATION ERRORS GENERATED FROM TWO PIXELS

(2): AVERAGED BINARIZATION ERROR

FIG. 3

(1): BINARIZATION ERRORS GENERATED FROM TWO PIXELS

(2): AVERAGED BINARIZATION ERROR

10: AVERAGING DEVICE

FIG. 4

(1): BINARIZATION ERROR INFORMATION-COMPRESSED BY CONVERTER

(2): EXPANDED BINARIZATION ERROR

(3): DIFFERENCE BETWEEN ORIGINAL BINARIZATION ERROR AND EXPANDED VALUE, I.E., BINARIZATION ERROR THAT CANNOT BE STORED IN BUFFER MEMORY

15: CONVERTER

16, 18: INVERSE CONVERTER

FIG. 5(a)

(1): BINARIZATION ERROR DATA INPUT FROM ADDER 2

(2): TO BUFFER MEMORY 3 AND INVERSE CONVERTER 16

(3): EXAMPLE OF CONVERTER 15

19: ONE- OR TWO-DIMENSIONAL LPF

20: DOWN-SAMPLING (THINNING)

FIG. 5(b)

(1): FROM BUFFER MEMORY 3 OR INVERSE CONVERTER 16

(2): TO ERROR FILTER 5 OR ADDER 17

(3): EXAMPLE OF INVERSE CONVERTERS 16 AND 18

21: INTERPOLATION

22: ONE- OR TWO-DIMENSIONAL LPF

FIG. 6

24: BIAS GENERATOR

FIG. 7

25: BINARY BUFFER MEMORY

26: TWO-DIMENSIONAL LPF

FIG. 8

(1): BINARIZATION ERROR (ALWAYS NONNEGATIVE)

28: ERROR DISTRIBUTOR

FIG. 9

(1): MOST SIGNIFICANT BIT

(2): LEAST SIGNIFICANT BIT

(3): BINARIZATION ERROR OF EACH PIXEL, WHICH IS READ OUT FROM BUFFER MEMORY

(4): BINARY EXPRESSION OF VALUE TO BE DISTRIBUTED TO HALFTONE IMAGE

(5): BINARY EXPRESSION OF BINARIZATION ERROR GENERATED FROM PIXEL b

(6): TO ADDER 6 IN FIG. 8

3: BUFFER MEMORY

FIG. 10

(1): HALFTONE IMAGE SIGNALS OF TWO PIXELS

(2): BINARY OUTPUT

30, 31, 32: COMPARATOR

33: SELECTOR

FIG. 11

(1): HALFTONE IMAGE SIGNAL

(2): BINARY OUTPUT

(3): PREDICTED VALUE (BINARY VALUE)

34, 35: COMPARATOR

36: SELECTOR

37: DELAY FOR ONE PIXEL

FIG. 12

38: DELAY FOR ONE LINE

FIG. 15

44: DELAY FOR ONE LINE

FIG. 16

(1): SIGNAL THAT CONTROLS SELECTOR

48: BINARY BUFFER MEMORY

49: PREDICTOR

FIG. 17

(1): HALFTONE IMAGE SIGNALS OF TWO PIXELS

(2): BINARY OUTPUT

50, 51: COMPARATOR

FIG. 18

(1): BINARY DATA OF REFERENCE LINE

(2): OUTPUT OF MR-ENCODED DATA

(3): BINARY DATA OF ENCODING LINE

25: BINARY BUFFER MEMORY

26: TWO-DIMENSIONAL LPF

55: MR ENCODER

FIG. 19

(1): PREDICTED VALUE (BINARY VALUE)

34, 35: COMPARATOR

36: SELECTOR

49: PREDICTOR

FIG. 20

(1): 0 OR 1 IS OUTPUT DEPENDING ON WHETHER VALUE OF PREDICTOR 49 COINCIDES WITH FINALLY OBTAINED BINARY IMAGE VALUE

(2): ENCODING OUTPUT

58: BINARY SIGNAL ENCODER

FIG. 21

(1): FROM ENCODER OUTPUT IN FIG. 20

(2): SIGNAL THAT CONTROLS SELECTOR 60

(3): BINARY IMAGE SIGNAL PREDICTED FROM VALUE STORED IN BINARY BUFFER MEMORY

(4): DECODED BINARY IMAGE SIGNAL

59: BINARY SIGNAL DECODER

60: SELECTOR

61: BINARY BUFFER MEMORY

62: PREDICTOR

FIG. 22(a)

205: BINARIZER

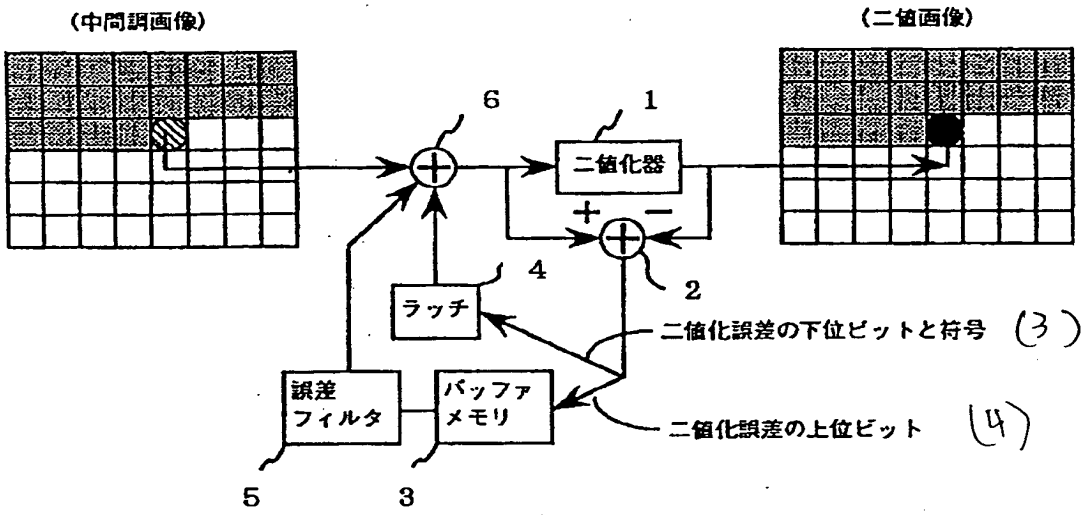
206: INTEGRATOR

FIG. 23

(1): BINARIZATION ERROR

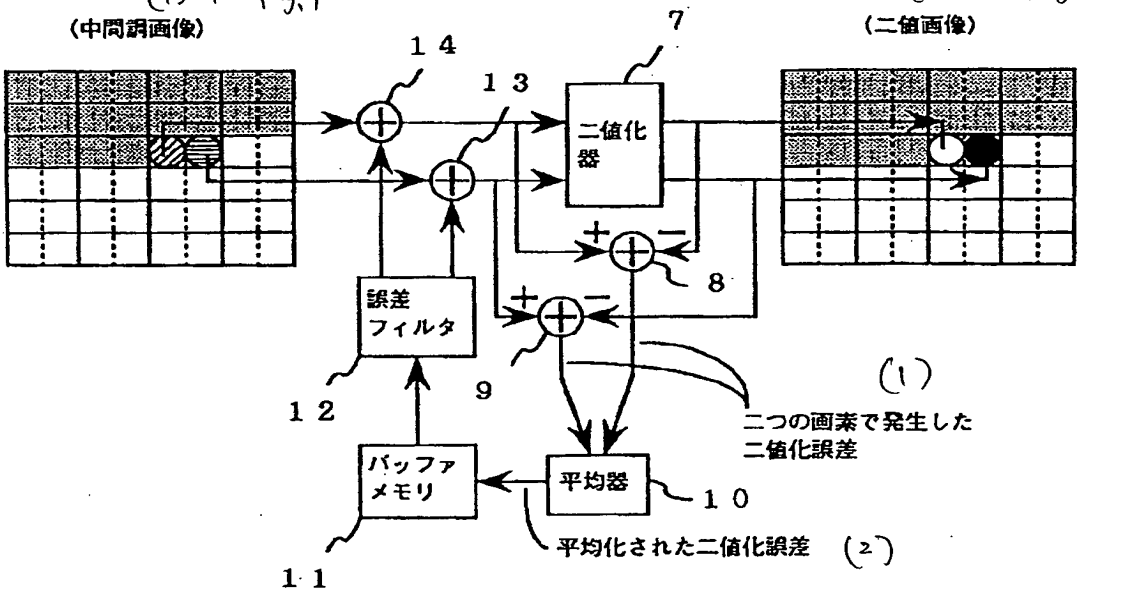
【図１】

【図１】　(1)　[Fig.1]　(2)



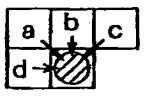
【図２】

【図２】　(1) in Fig.1　[Fig.2]　(2) in Fig.2



【図２４】　[Fig.24]

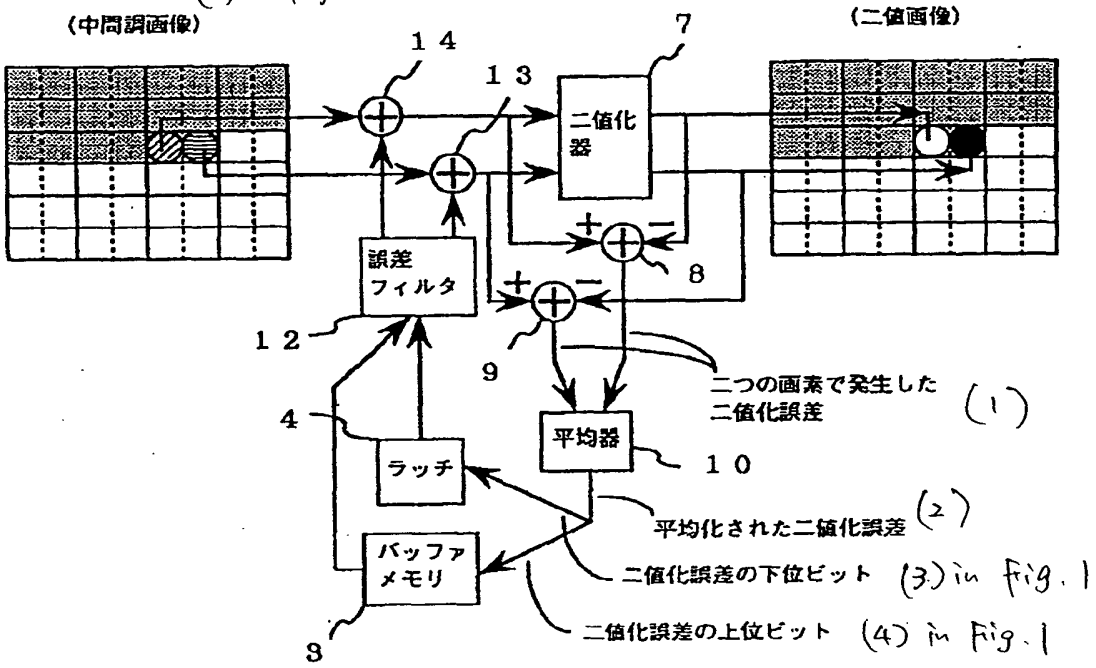
【図２４】



【図３】

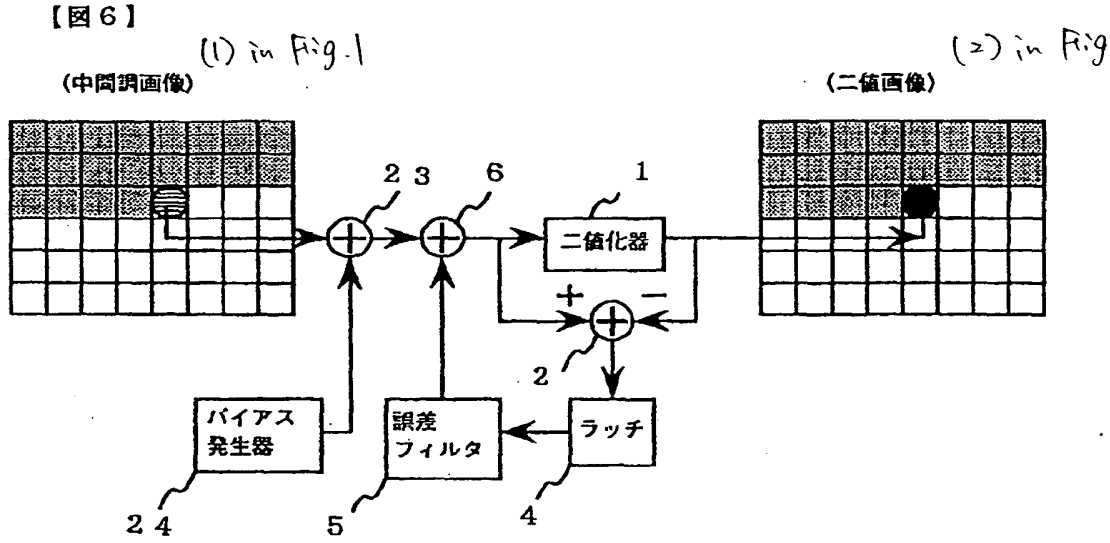
【図３】

[Fig.3]



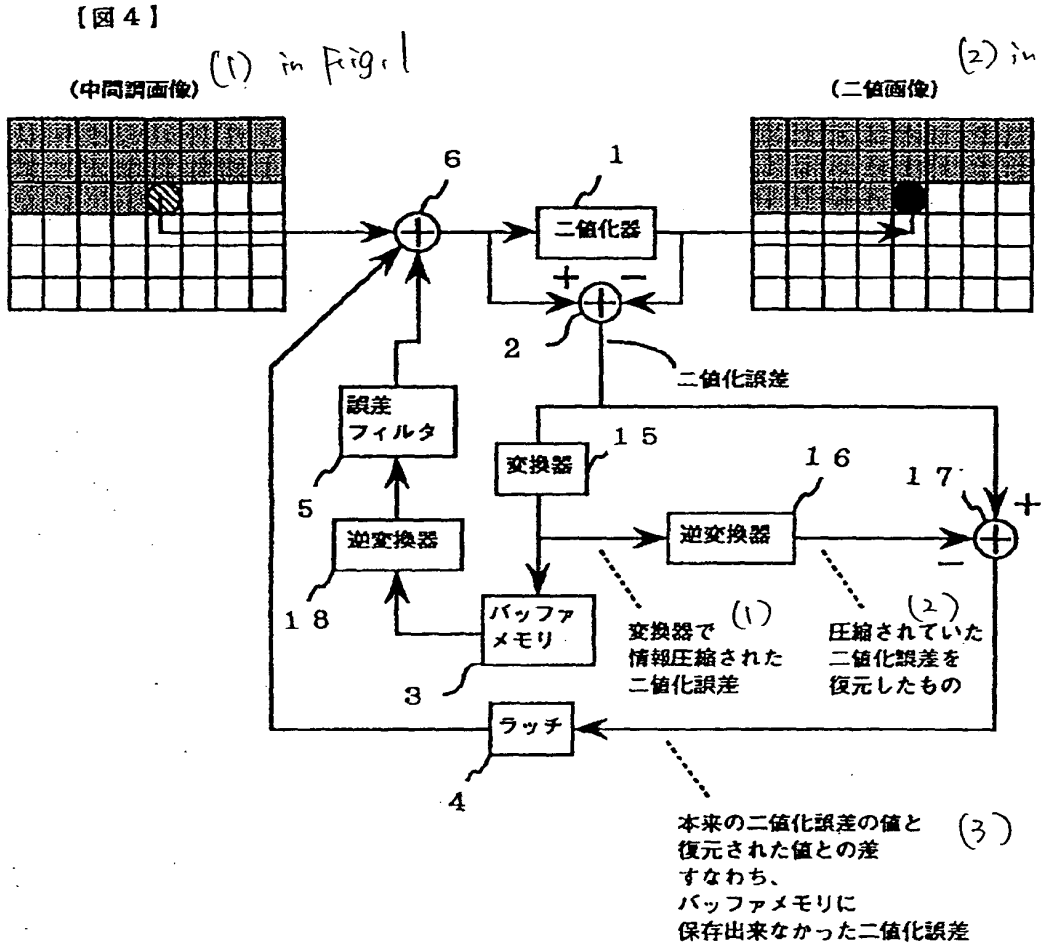
[Fig.6] 【図６】

【図６】



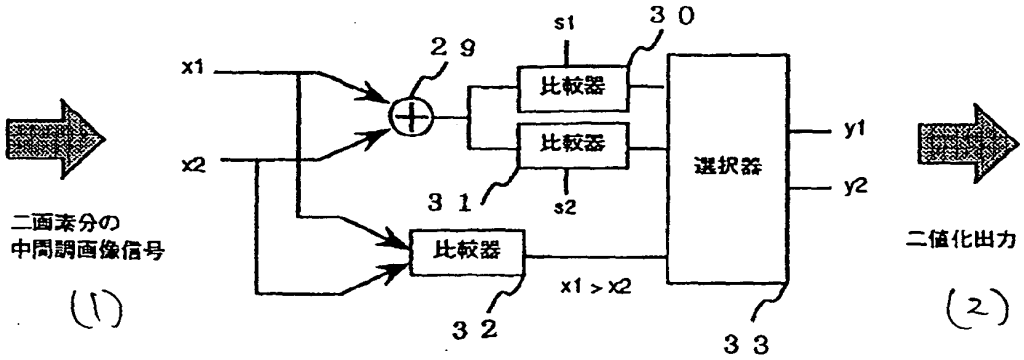
[Fig.4] 【図４】

【図４】



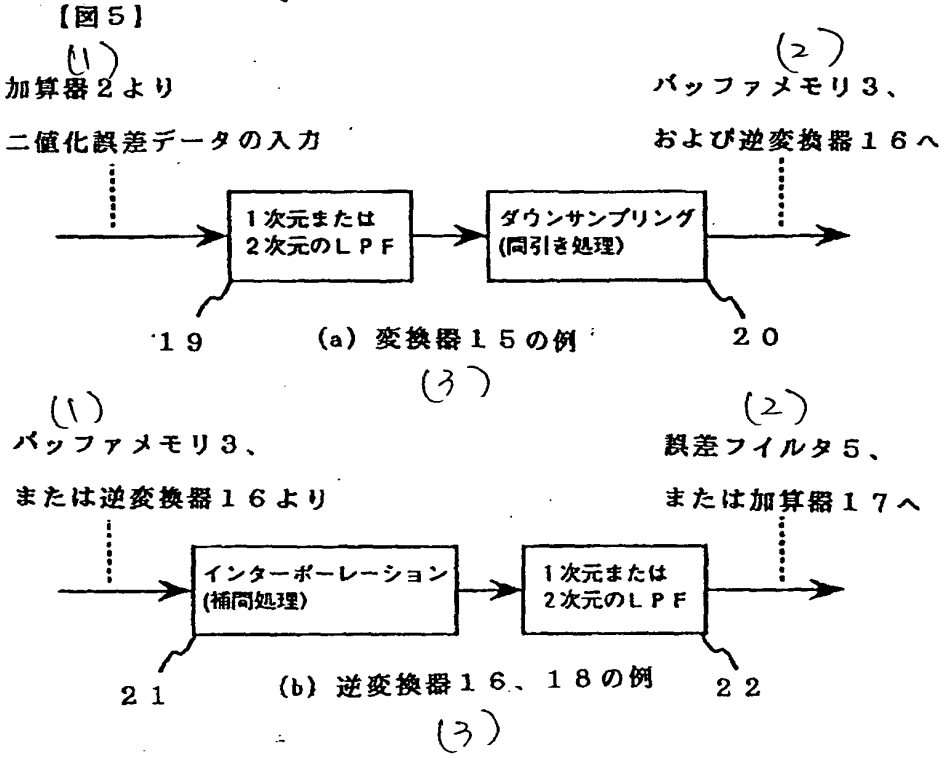
[Fig.10] 【図１０】

【図１０】



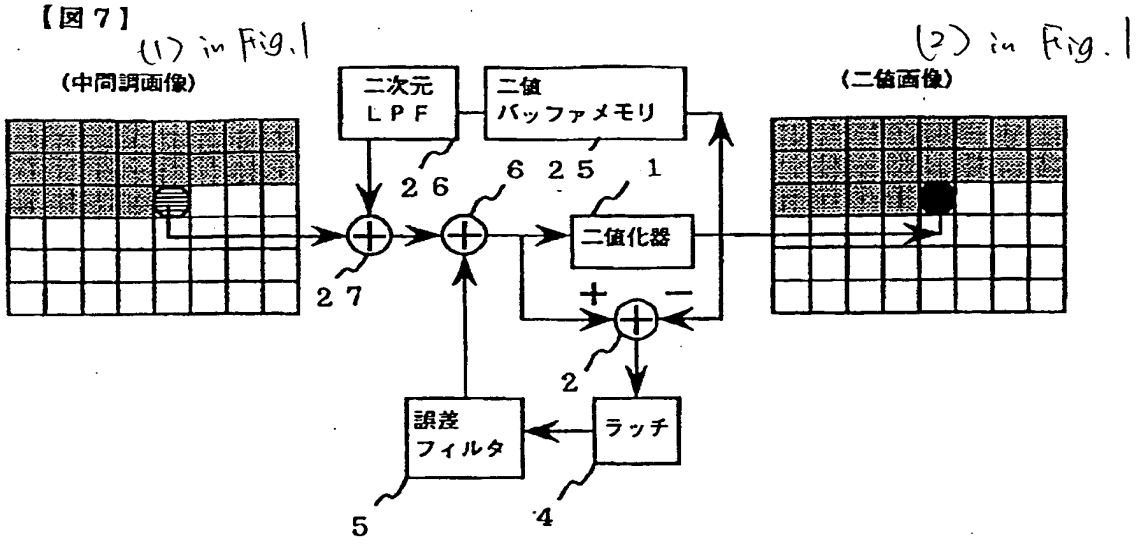
[Fig. 5]　【図５】

【図５】


(1)
加算器２より
二値化誤差データの入力
(2)
バッファメモリ３、
および逆変換器１６へ
１次元または
２次元のＬＰＦ
ダウンサンプリング
(間引き処理)
１９
(a) 変換器１５の例
２０
(3)
(1)
バッファメモリ３、
または逆変換器１６より
(2)
誤差フイルタ５、
または加算器１７へ
インターポーレーション
(補間処理)
１次元または
２次元のＬＰＦ
２１
(b) 逆変換器１６、１８の例
２２
(3)

[Fig.7]　【図7】

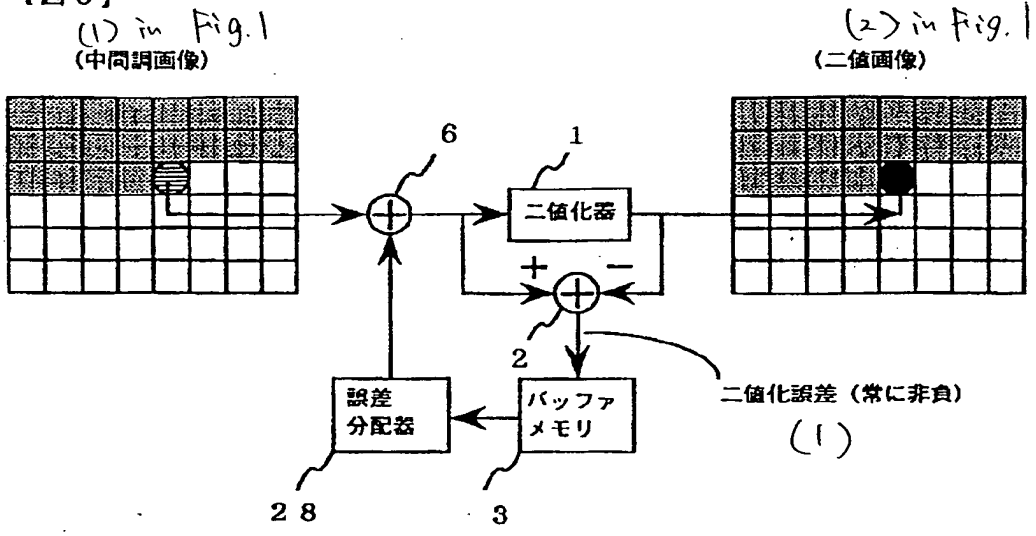
【図7】



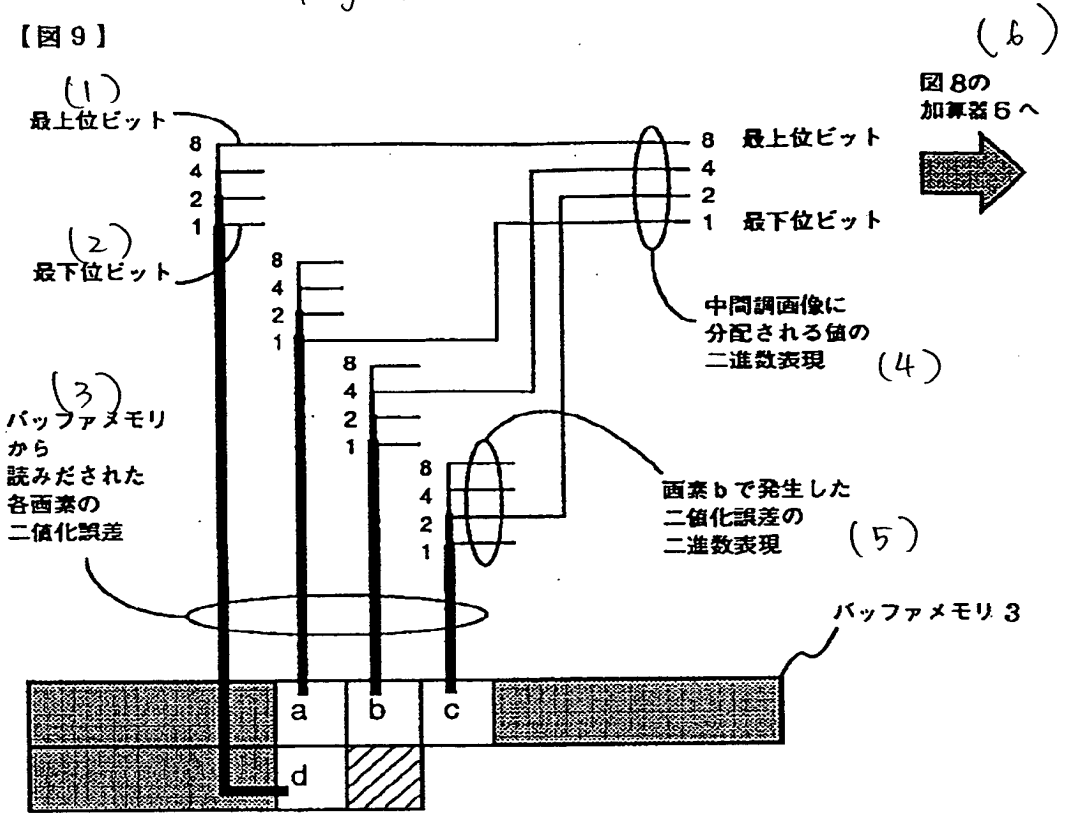
【図8】

[Fig.8]

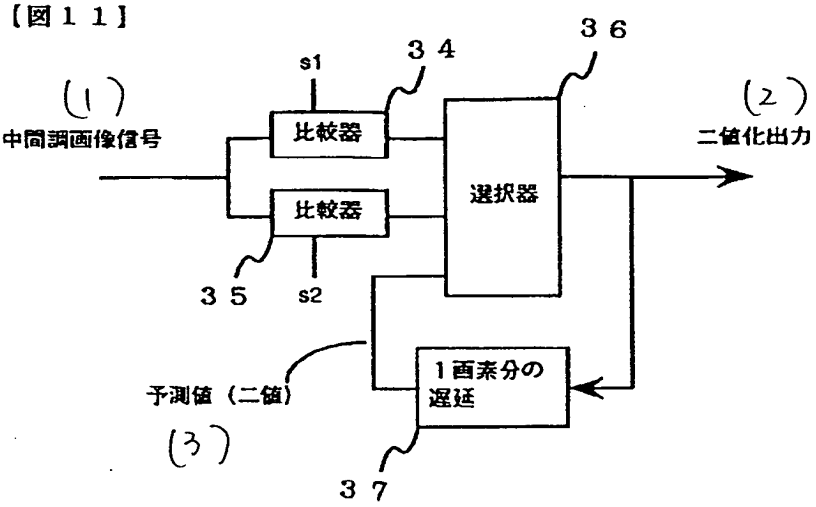
【図8】



[Fig. 9]　【図９】

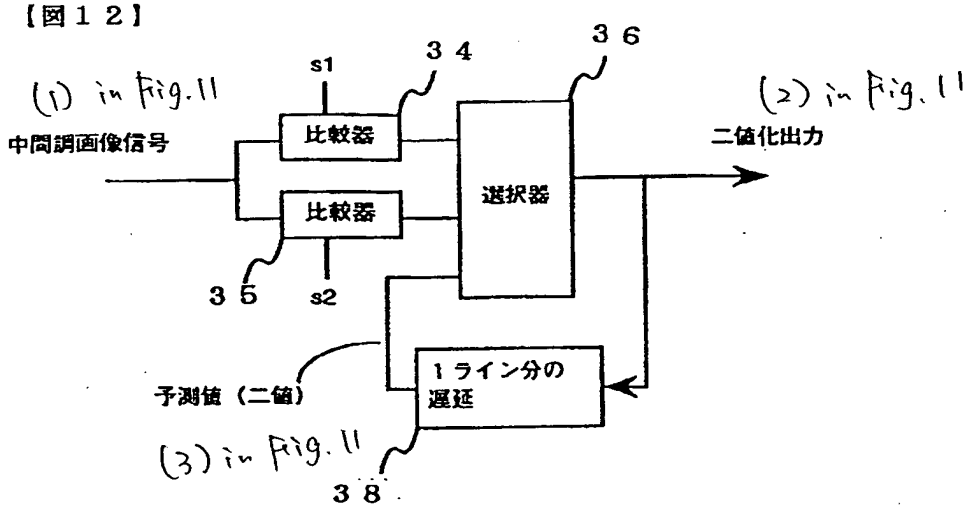


[Fig. 11]　【図１１】



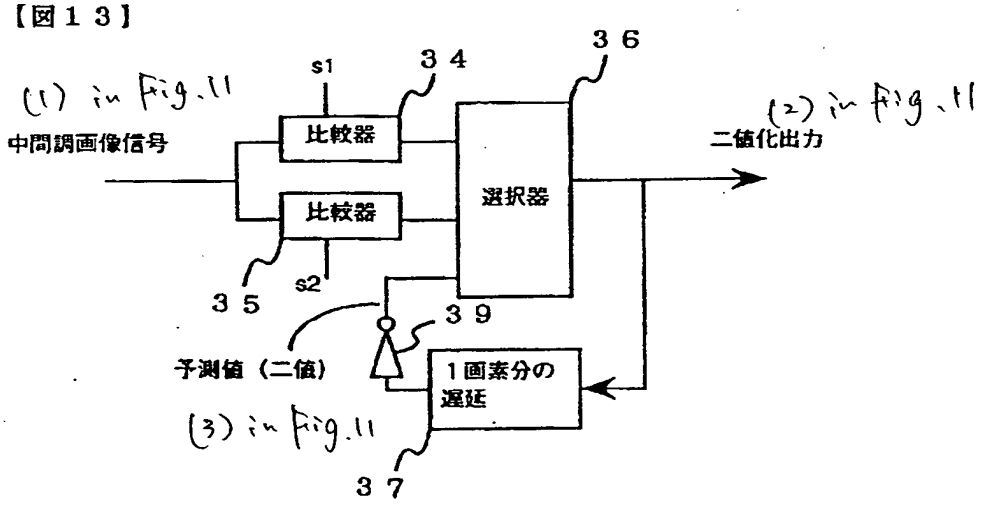
[Fig.12] 【図１２】

【図１２】



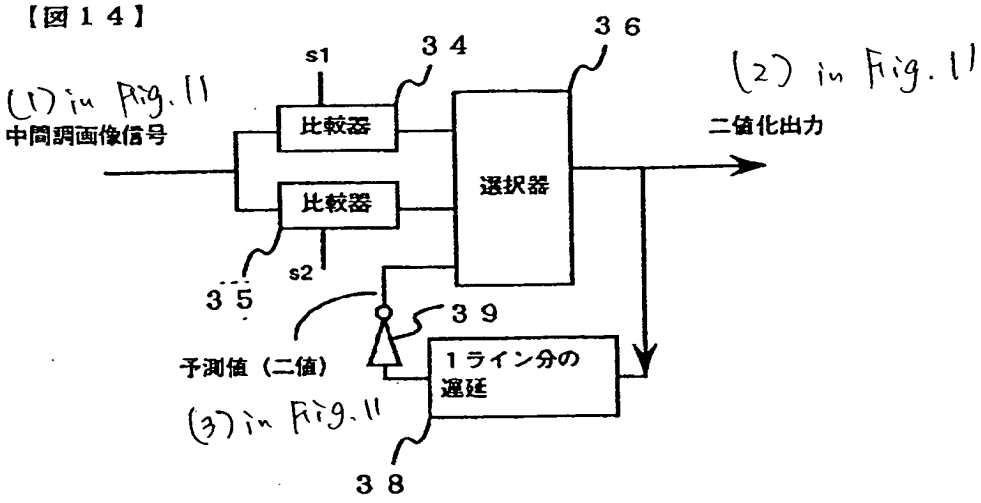
[Fig.13] 【図１３】

【図１３】



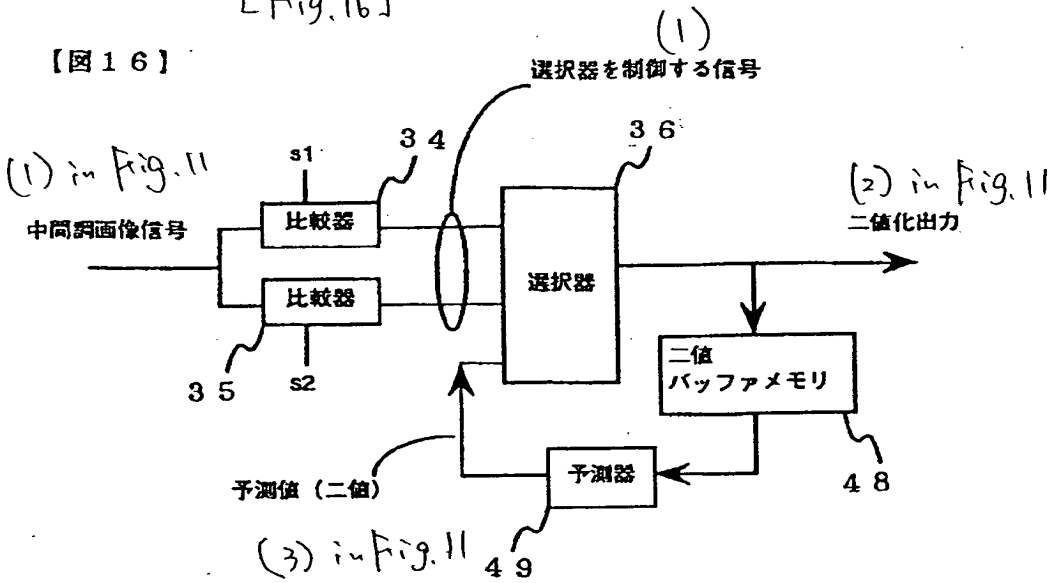
[Fig.14] 【図１４】

【図１４】



[Fig.16] 【図１６】

【図１６】

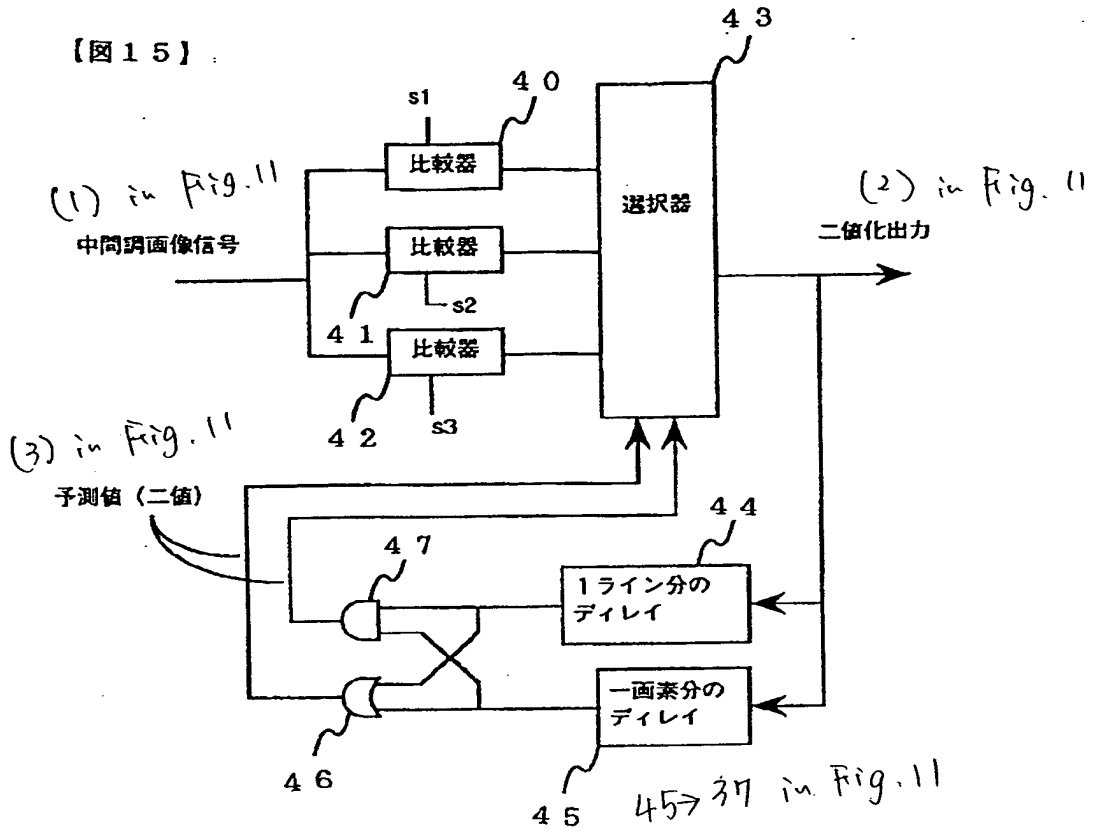


【図１５】

[Fig.15]

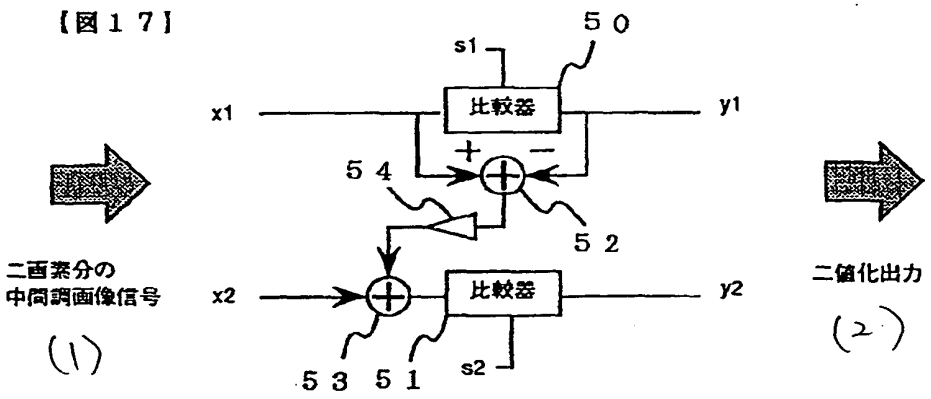
40,41,42 → 34 in Fig.11

43 → 36 in Fig.11



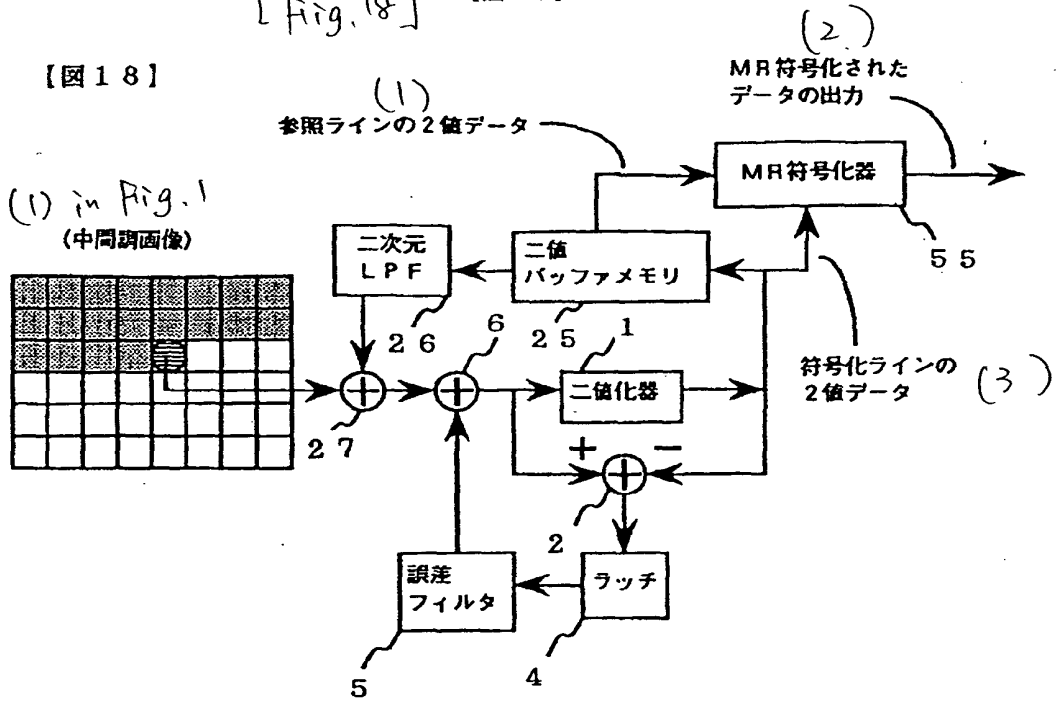
[Fig.17] 【図１７】

【図１７】

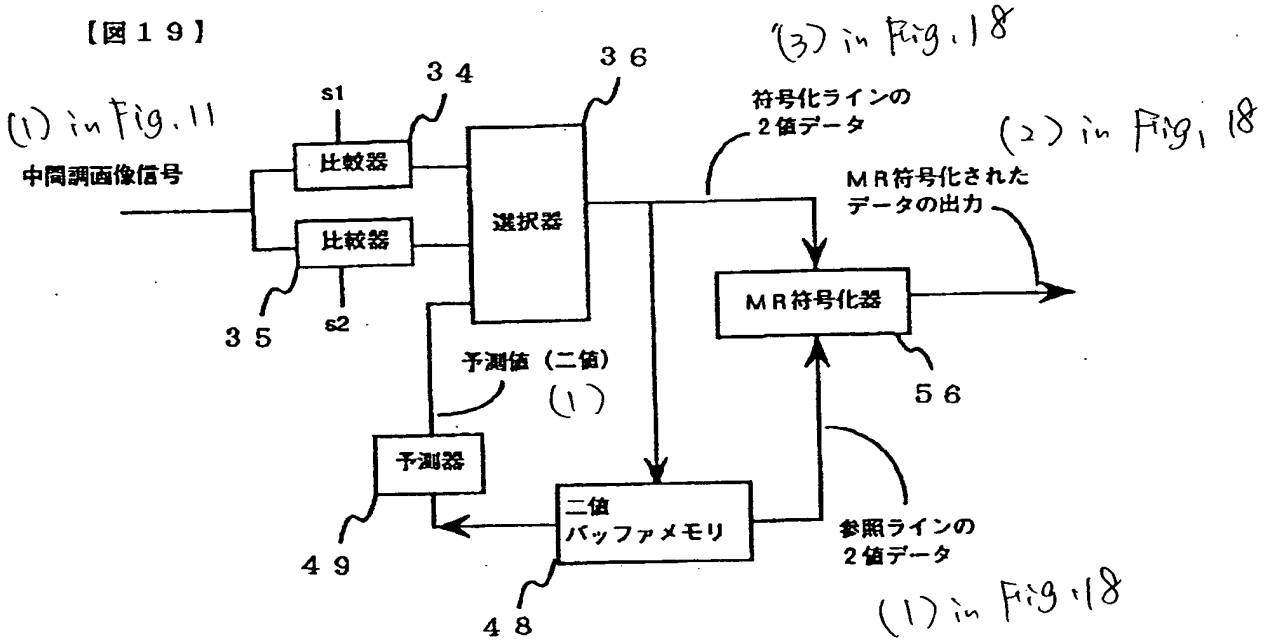


[Fig.18] 【図１８】

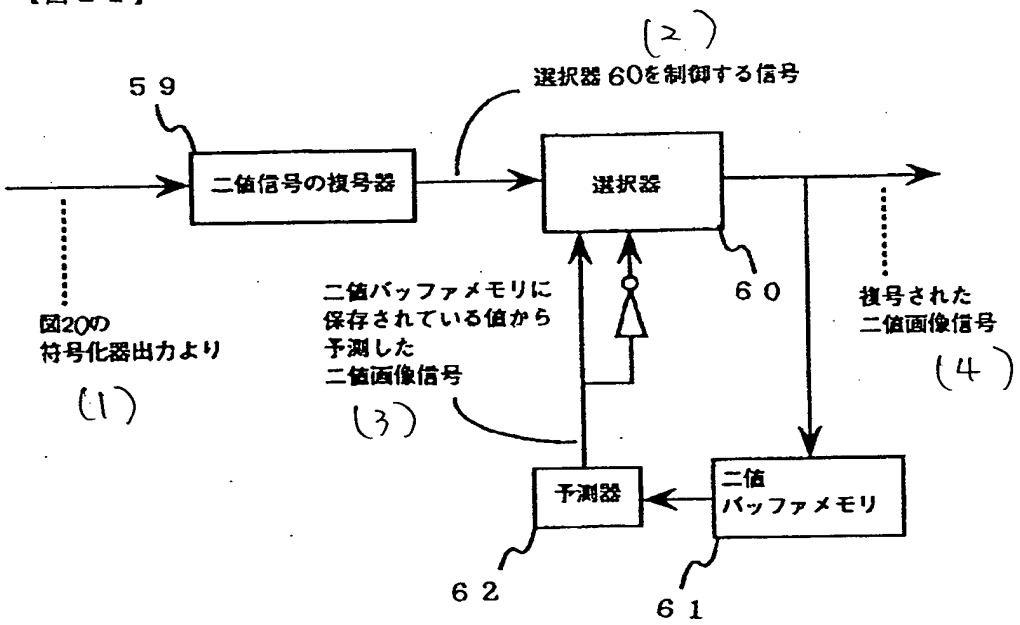
【図１８】



[Fig.19] 【図１９】

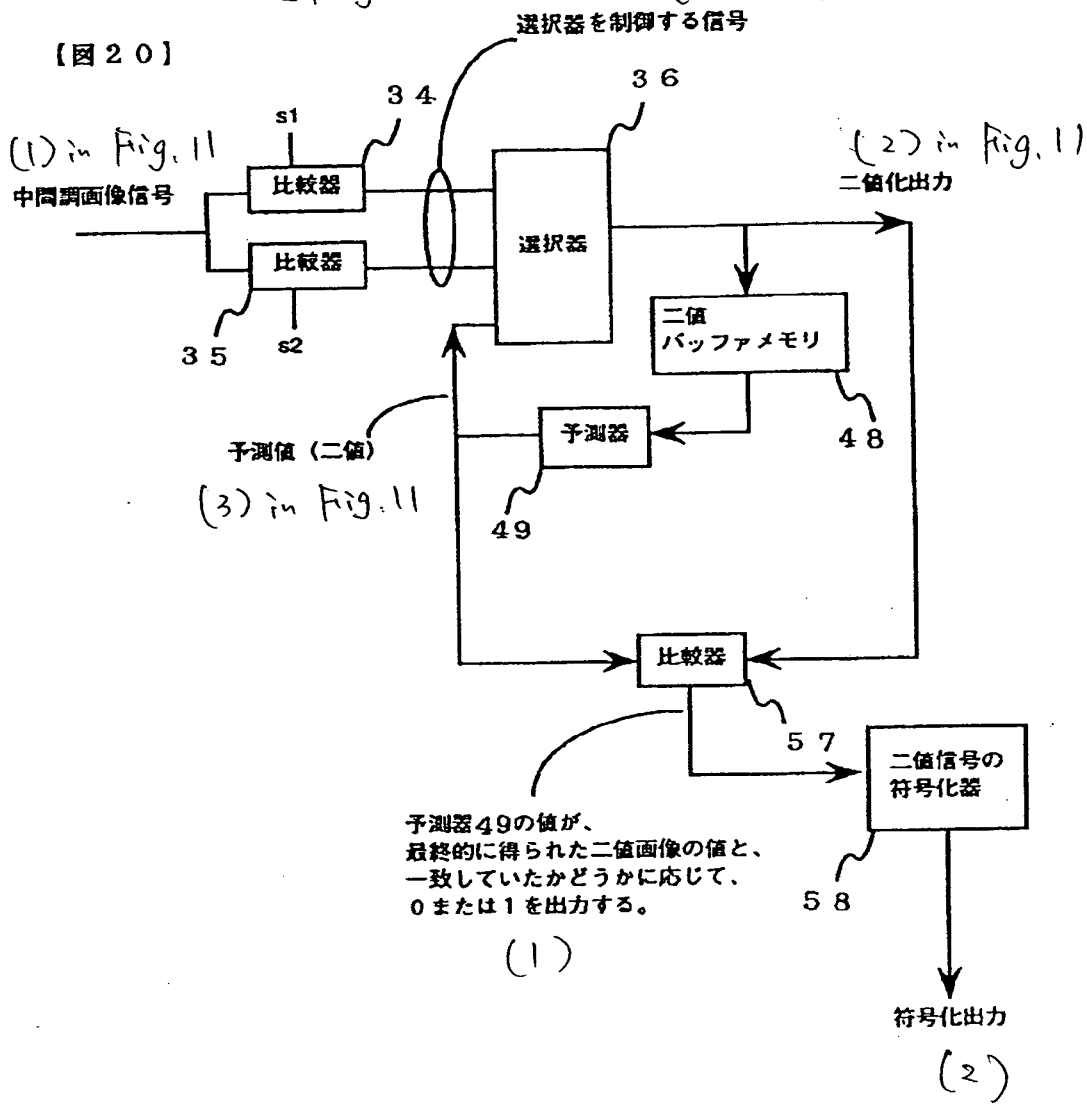


[Fig.21] 【図２１】



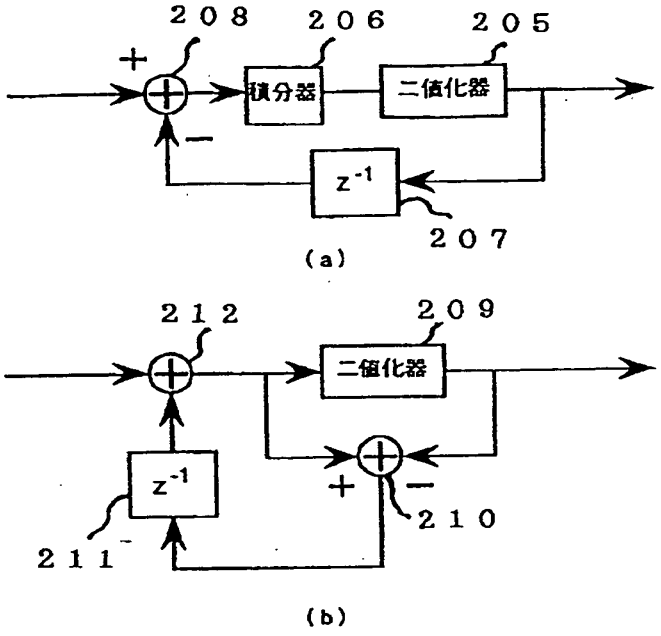
【図２０】

[Fig.20]　【図２０】　(1) in Fig.16



[Fig.22] 【図２２】

【図２２】



【図２３】

[Fig.23]

【図２３】